AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) A circuit for reducing the number of bits in a data value, the circuit comprising:

a first summing circuit configured to add an error offset value and one or more ~~MSBs~~ most significant bits (MSBs) of said bit

5   data value to produce a result data value;

a control circuit configured to generate a dither offset value;

an error feedback circuit configured to receive one or more ~~LSBs~~ least significant bits (LSBs) of said result data value

10   and generate an error value dependent on said LSBs;

a second summing circuit configured to add said dither offset value and said error value to provide said error offset value; and

a processor configured to selectively control generation

15   of said dither offset value and said error value.

2. (ORIGINAL) The circuit according to claim 1, wherein said data value is representative of a pixel data for display on a video display screen.

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3.   (ORIGINAL) The circuit according to claim 2, wherein said control circuit comprises:

a dither generating circuit configured to generate said dither offset value in response to the LSBs of each of a first and

5.   second coordinates of said pixel data represented by said data value.

4.   (ORIGINAL) The circuit according to claim 3, wherein:

said dither generating circuit comprises first and second inputs; and

5   said control circuit comprises:

a first coordinate counter for counting through said first coordinates from a first initial value and applying the LSBs of each said first coordinates to said first input of said dither generating circuit; and

10   a second coordinate counter for counting through said second coordinates from a second initial value and applying the LSBs of each said second coordinates to said second input of said dither generating circuit, wherein each of said first and second coordinate counters comprises a reset input for resetting to

15   said first and second initial values in response to receipt of a respective reset signal.

5. (ORIGINAL) The circuit according to claim 4, wherein:

said first counter reset signal comprises a horizontal synchronization signal; and

said second counter reset signal comprises a vertical synchronization signal.

6. (ORIGINAL) The circuit according to claim 5, wherein said horizontal synchronization signal is further configured to increment said second coordinate counter.

7. (ORIGINAL) The circuit according to claim 1, wherein said processor is further configured to generate a preselected concealment type signal for controlling generation of said dither offset value and said error value.

8. (ORIGINAL) The circuit according to claim 7, wherein said control circuit further comprises:

a dither offset generating circuit operable to generate said dither offset value in dependence on said preselected concealment type signal; and

an inhibit circuit for inhibiting said error value in response to said preselected concealment type signal.

9.   (ORIGINAL) The circuit according to claim 1, further

comprising:

     a truncation circuit for truncating said data value to a

predetermined bit value and applying said predetermined bit value

5   to said first summing circuit.

10.   (CURRENTLY AMENDED) The circuit according to claim

1, further comprising:

     a limit circuit for receiving a first <u>set of most

significant bits (MSBs)</u> ~~MSBs~~ from said first summing circuit and

5   generating a bit output of a value in response to the value of the

MSB of said first MSBs.

11.   (CURRENTLY AMENDED) A method of applying error

concealment to the reduction of a data value, comprising the steps

of:

     (A)   receiving a series of successive data values;

5   (B)   generating a respective error offset value for each

of said data values; and

     (C)   adding each of said error offset values to a <u>one or

more most significant bits (MSBs)</u> ~~MSBs~~ of the next following data

value to produce a respective result value<u>, wherein step (B)

10   further comprises the sub-steps of (B-1) generating a dither offset

value for each of said data values, (B-2) generating an error value</u>

from one or more least significant bits (LSBs) of the previous result value, and (B-3) summing said dither offset value and said error value to produce said error offset value.

12.   (CANCELED)

13.   (ORIGINAL) The method according to claim 11, wherein said data value is representative of a pixel data for display on a video display screen.

14.   (CURRENTLY AMENDED) The method according to claim 13, wherein step (B) further comprises:

generating said dither offset value in response to the LSBs of each of a first and a second ~~coordinates~~ coordinate of said pixel data represented by said data value.

15.   (ORIGINAL) The method according to claim 14, wherein said dither offset value is a function of the LSBs of each said first and second coordinate of said pixel data.

16.   (ORIGINAL) The method according to claim 15, wherein step (B) further comprises:

counting through said first coordinates from a first initial value;

counting through said second coordinates from a second

initial value; and

generating said dither offset values in response to the

LSBs of each said first and second coordinates.

17.   (ORIGINAL)   The   method   according   to   claim   16,

wherein:

said   first   coordinate   is   reset   by   a   horizontal

synchronization signal;

said   second   coordinate   is   reset   by   a   vertical

synchronization signal.

18.   (CURRENTLY AMENDED) The method according to claim 11

~~12~~, wherein step (B) further comprises:

generating   a   preselected   concealment   type   signal   for

controlling generation of said dither offset value and said error

value.

19.   (ORIGINAL) The method according to claim 11, wherein

step (C) further comprises:

generating a bit output of a value dependent on the value

of the MSB of said result value.

20. (CURRENTLY AMENDED) The method according to claim <u>11</u> ~~12~~, wherein step (B) further comprises:

generating a concealment type signal; and

generating said dither offset value in dependence on said

5. concealment type signal.